IN THE CLAIMS:

Claim 1 (currently amended): A multiprocessor array which includes: a) a first processor shadow register unit (1) which operates within a first clock domain and includes i) a first processor (2), and ii) a first shadow register unit (3) which is connected to the first processor (2) so as to transmit data bidirectionally, b) at least one second processor shadow register unit (9) which i) operates within a corresponding second clock domain, ii) includes a second processor (10), and iii) a second shadow register unit (11) which is connected to the second processor (10) so as to transmit data bidirectionally, and c) a peripheral unit (17) which operates within a peripheral clock domain and includes i) a multiplexer unit (18) which is connected to the first shadow register unit (3) and the at least one second shadow register unit (11) so as to transmit data bidirectionally, ii) a register unit (20)[[,]] having the construction of the first shadow register unit (3) and the at least one second shadow register unit (11) and the register unit (20) being identical in respect of function, and iii) a priority unit (19) directly connected to a multiplexer unit (18) via only a single active connection for applying control signals thereto and for allocating the multiplexer unit (18) for data transmission to the first shadow register unit (3) or to the at least one second shadow register unit (11) based on at least one criterion, the priority unit (19) being connected to the first shadow register unit (3) and to the at least one second shadow register unit (11), via a corresponding asynchronous request line, said request line informing the priority unit of changes in a corresponding shadow register.

Claim 2 (original): A multiprocessor array as claimed in claim 1, characterized in that the first shadow register unit (3), the at least one second shadow register unit (11) and the register unit (20) include status flags as well as control/data registers.

Claim 3 (previously presented): A multiprocessor array as claimed in claim 1, characterized in that the first clock domain and/or the at least one second clock domain include more than one processor.

Claim 4 (previously presented): A multiprocessor array as claimed in claim 1, characterized in that in order to read out data from the first shadow register unit (3) and/or the at least one second shadow register unit (11) the multiplexer unit (18) is connected thereto in the read out direction.

Claim 5 (previously presented): A multiprocessor array as claimed in claim 1, characterized in that requests for access from the first shadow register unit (3) and/or the at least one second shadow register unit (11) to the priority unit (19) are encoded as a one-bit signal.

Claim 6 (previously presented): A multiprocessor array as claimed in claim 1, wherein said at least one criterion is in conformity with the principle: first-come, first-served.

Claim 7 (previously presented): A multiprocessor array as claimed in claim 1, wherein said at least one criterion is in conformity with the principle: all shadow register units (3, 11) are served successively.

Claim 8 (previously presented): A multiprocessor array as claimed in claim 1, wherein said at least one criterion is in conformity with the principle: each shadow register unit is statistically allocated a given percentage of the time for accessing the peripheral unit

(17).

Claim 9 (previously presented): A multiprocessor array as claimed in claim 1, characterized in that the peripheral unit (17) is constructed as an infrared interface, UART interface or USB interface.

Claim 10 (currently amended): A multiprocessor array as claimed in claim 1, characterized in that the first shadow register unit (3) and/or the at least one second shadow register unit (11) ~~are~~ are connected to the associated processor (2, 10) via an interrupt (8, 16) initiated by respective status flags of said first and second shadow register units.

Claim 11 (currently amended): A communication terminal using a multiprocessor array comprising: a) a first processor shadow register unit (1) which operates within a first clock domain and includes i) a first processor (2), and ii) a first shadow register unit (3) which is connected to the first processor (2) so as to transmit data bidirectionally, b) at least one second processor shadow register unit (9) which i) operates within a corresponding second clock domain, ii) includes a second processor (10), and iii) a second shadow register unit (11) which is connected to the second processor (10) so as to transmit data bidirectionally, and c) a peripheral unit (17) which operates within a peripheral clock domain and includes i) a multiplexer unit (18) which is connected to the first shadow register unit (3) and the at least one second shadow register unit (11) so as to transmit data bidirectionally, ii) a register unit (20)[[,]] having the construction of the first shadow register unit (3) and the at least one second shadow register unit (11) and the register unit

(20) being identical in respect of function, and iii) a priority unit (19) directly connected to a multiplexer unit (18) via only a single active connection for applying control signals thereto and for allocating the multiplexer unit (18) for data transmission to the first shadow register unit (3) or to the at least one second shadow register unit (11) based on at least one criterion, the priority unit (19) being connected to the first shadow register unit (3) and to the at least one second shadow register unit (11), via a corresponding asynchronous request line, said request line informing the priority unit of changes in a corresponding shadow register.

Claim 12 (currently amended): A portable device using a multiprocessor array comprising: a) a first processor shadow register unit (1) which operates within a first clock domain and includes i) a first processor (2), and ii) a first shadow register unit (3) which is connected to the first processor (2) so as to transmit data bidirectionally, b) at least one second processor shadow register unit (9) which i) operates within a corresponding second clock domain, ii) includes a second processor (10), and iii) a second shadow register unit (11) which is connected to the second processor (10) so as to transmit data bidirectionally, and c) a peripheral unit (17) which operates within a peripheral clock domain and includes i) a multiplexer unit (18) which is connected to the first shadow register unit (3) and the at least one second shadow register unit (11) so as to transmit data bidirectionally, ii) a register unit (20)[[,]] having the construction of the first shadow register unit (3) and the at least one second shadow register unit (11) and the register unit (20) being identical in respect of function, and iii) a priority unit (19) directly connected to a multiplexer unit (18) via only a single active connection for applying control signals thereto and for allocating the multiplexer unit (18) for data transmission to the first shadow register unit (3) or to the at

least one second shadow register unit (11) based on at least one criterion, the priority unit (19) being connected to the first shadow register unit (3) and to the at least one second shadow register unit (11), via a corresponding asynchronous request line, said request line informing the priority unit of changes in a corresponding shadow register.